

In the Claims:

Please cancel claim 8 without prejudice or disclaimer.

Please amend claims 1-2 and 9 as follows:

Claim 1 (currently amended) A method for manufacturing a semiconductor device, comprising:

- a) forming a contact hole to expose a joining portion by etching an inter-layer insulation layer disposed on top of a semiconductor substrate;
- b) forming a contact plug inside the contact hole;
- c) molding an etch stop layer and a sacrificial oxide layer on the contact plug and the inter-layer insulation layer;
- d) molding a storage node hole to expose the contact plug by etching the etch stop layer and the sacrificial oxide layer;
- e) molding a silicide layer on the contact plug;
- e) ~~f)~~ f) forming a TiN bottom electrode comprising a ~~TiN~~ TiN layer inside the storage node hole by a CVD method;
- ~~f)~~ g) separating the TiN bottom electrode by removing the TiN layer;
- ~~g)~~ h) exposing the TiN bottom electrode ~~pattern~~ by removing the sacrificial oxide layer;
- ~~h)~~ i) forming a dielectric layer on the TiN bottom electrode pattern; and
- ~~i)~~ j) molding a top electrode on the dielectric layer.

Claim 2 (currently amended) The method as recited in claim 1, wherein part b) further comprises:

- forming a the contact hole by etching the inter-layer insulation layer ~~optionally~~; and
- depositing a conductor layer inside the contact hole and leveling the conductor layer.

Claim 3 (original) The method as recited in claim 2, wherein the depositing and leveling of the conductor layer is carried out with a CMP or an etch back.

Claim 4 (original) The method as recited in claim 1, wherein the etch stop layer comprises a material selected from the group consistency of SiN, Al₂O₃, SiON and Si₃N₄.

Claim 5 (original) The method as recited in claim 1, wherein at part d) of forming the storage node hole, the sacrificial oxide layer and the etch stop layer are dry etched.

Claim 6 (original) The method as recited in claim 1, wherein at part d) of forming the storage node hole, the inter-layer insulation layer around the contact plug is exposed.

Claim 7 (original) The method as recited in claim 1, wherein the contact plug comprises of polysilicon.

Claim 8 (currently canceled)

Claim 9 (currently amended) The method as recited in claim 8 1, wherein the step of forming the silicide layer further comprises:

depositing a metallic layer selected from the group consisting of Ti, Co and Ni on top of the semiconductor substrate where the storage node hole is molded; and
forming the silicide layer selected from the group consisting of TiSi_2 , CoSi_2 and NiSi_2 on the contact plug by thermally treating the metallic layer.

Claim 10 (original) The method as recited in claim 9, further comprising the step of removing any metallic layer not connected to a silicide layer and that remains after the step of forming the silicide layer.

Claim 11 (original) The method as recited in claim 10, wherein at the step of removing the metallic layer, the metallic layer is removed in a cleaning process using a mixture of H_2SO_4 and H_2O_2 .

Claim 12 (original) The method as recited in claim 1, wherein at the step of separating the TiN bottom electrode neighboring the sacrificial oxide layer, the TiN layer is removed in the chemical-mechanical polishing method until the sacrificial oxide layer is exposed.

Claim 13 (original) The method as recited in claim 1, wherein the dielectric layer is selected from the group consisting of BST, STO, PZT, PLZT, SBT, TaON and Ta₂O₅.

Claim 14 (original) The method as recited in claim 1, wherein the top electrode is selected from the group consisting of TiN, Ru, Pt, Ir, Os, W, Mo, Co, Ni, Au, Ag, RuO₂ or IrO₂.

Claim 15 (original) A semiconductor device comprising a capacitor made in accordance with the method of claim 1.

Claim 16 (original) A semiconductor device comprising a capacitor made in accordance with the method of claim 3.

Claim 17 (original) A semiconductor device comprising a capacitor made in accordance with the method of claim 11.